Improvement of Fixed Pattern Noise and Electrical Cross-Talk in Small-Sized Pixel-Parallel ADCs

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***Abstract*— This paper introduces the phenomenon and underlying causes of fixed pattern noise (FPN) and electrical cross-talk (XT) in small-sized pixel-parallel ADC and proposes an effective method to address these issues. Pixel-parallel ADC is a promising architecture that enhances key image sensor performance, including frame rate, noise, dynamic range, and power efficiency, compared to conventional column-parallel ADCs. Despite these advantages, the large size of the digital pixels remains a significant challenge, limiting its practical applicability and value. To reduce pixel size, we proposed a cluster-based structure. However, this approach introduced two major issues: cluster-induced fixed pattern noise (CL-FPN) in dark conditions and cluster-induced cross-talk (CL-XT) in illuminated conditions. CL-FPN arises due to dark offset errors in the M×N cluster configuration. On the other hand, CL-XT occurs at the boundary between bright and dark regions, where the output code value of a bright pixel inadvertently affects adjacent dark pixels, a causing them to appear as white pixels. To identify the root causes of these issues, we performed precise circuit simulations and related measurements. Ultimately, we successfully mitigated the problems, and the simulation results were confirmed to align closely with the package measurements of digital pixel sensor (DPS).**

Keywords—CMOS Image sensor, global shutter, pixel-parallel ADC, pixel-level ADC, digital pixel sensor, cluster structure, cluster induced fixed pattern noise, cluster induced cross-talk

I. INTRODUCTION

Recently, global-shutter (GS) CMOS image sensors (CISs) have gained widespread adoption in various applications, including automotive cameras, machine vision (MV), augmented reality (AR), and so on. In particular, high-performance GS CIS with features such as high speed, low noise, and low power consumption is in high demand, especially for flagship camera applications. One promising solution to meet these requirements is a digital pixel sensor (DPS). In this paper, we present a shrinkage technology for DPS, incorporating an in-pixel analog-to-digital converter (ADC) with memory. Additionally, we address the potential side effects of the proposed shrinkage method and discuss effective solutions to mitigate these issues. To enhance sensor performance, the digital pixel includes a size-optimized pixel-parallel ADC (P-ADC) and digital memories for storing the converted pixel data. As shown in Fig. 1, the proposed sensor architecture performs A/D conversion globally using P-ADCs. This approach offers several advantages: 1) high-speed data readout in the digital domain, 2) low-noise performance due to slower ADC operation compared to the conventional architecture, and 3) low-power consumption achieved by longer blank time in the analog domain. Despite these benefits, the relatively large pixel size of the digital pixels remains a critical challenge, limiting their applicability and value. To address this issue, we investigated methods to shrink and optimize the digital pixel size and proposed a cluster-based structure. As illustrated in Fig. 2, the digital pixel is designed with a 2-layer structure (top layer: photodiode, bottom layer: ADC and memory), and to eliminate unnecessary area, the analog circuits on the bottom layer are effectively integrated into the corresponding M×N pixel area, thereby defining the cluster structure.

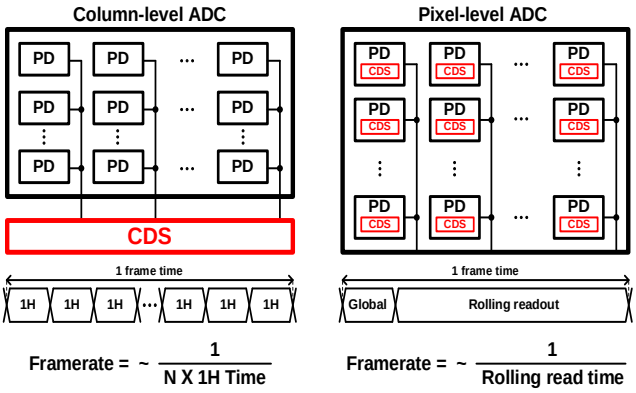


Fig.1 Sensor architectures of (a) Column-level ADC, and (b) Pixel-level ADC.

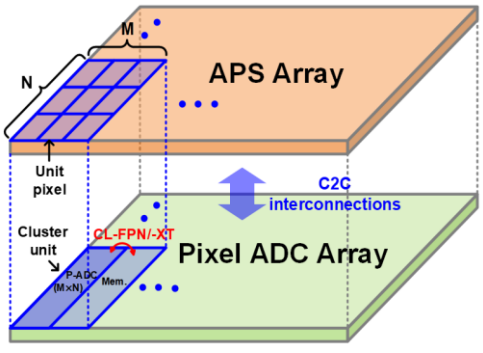


Fig.2 Block diagram of 2-stack DPS with cluster structure.

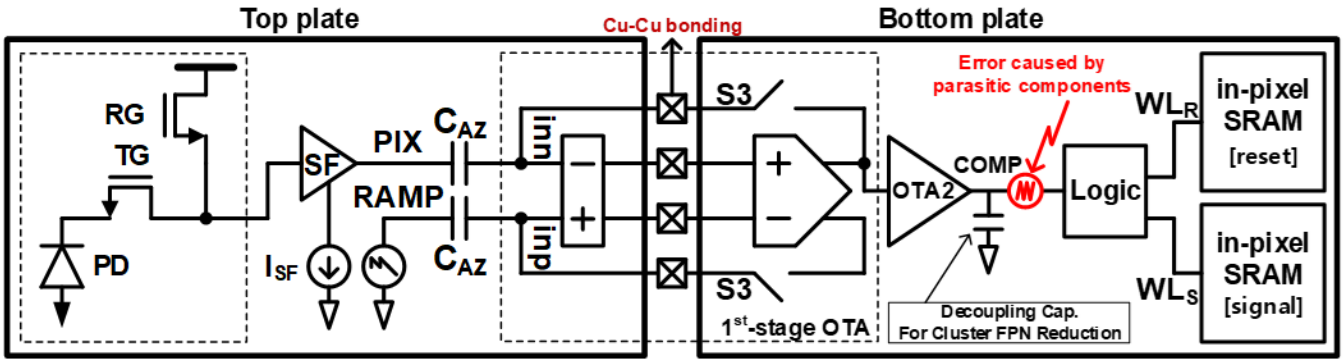


Fig. 3 Simplified clustered unit and pixel-parallel ADC circuit diagram with the parasitic components.

The complex cluster structure, however, introduces two critical issues: 1) cluster-induced fixed pattern noise (CL-FPN) under dark conditions, and 2) cluster-induced cross-talk (CL-XT) under illuminated conditions.

This paper has been validated through precise simulations incorporating parasitic components and further demonstrated with measurement results. The remainder of the paper is organized as follows. Section II discusses the causes of CL-FPN and CL-XT, along with proposed solutions. Section III presents the simulation and measurement results after optimizing the parasitic components. Finally, the conclusion is given in Section IV.

II. The Causes and Solutions

The CL-FPN issue refers to dark offset errors occurring in the M×N cluster structure. As shown in Fig 3, the primary cause of CL-FPN is capacitive coupling between the adjacent ADC output node, COMP and SRAM input node, WL. This issue is further illustrated in Fig 4. When two adjacent pixels PIX<A> and PIX<B> are in the same dark condition, PIX<A> is first converted into a digital code by the ADC, which consists of OTA1 and OTA2. This conversion occurs at the decision point when the pixel output and ramp output intersect at the zero-crossing point, and the digital code is stored in the SRAM. During this process, the COMP<A> node switches from low to high, and then the WL<A> node switches from high to low. At that time, the PIX<B> undergoes a similar operation. Unfortunately, WL_R<B> and WL_S<B> parasitically couple to COMP<A>, causing different errors during the reset and signal intervals, ultimately resulting in dark offset errors. This phenomenon is defined as CL-FPN. Basically, capacitive coupling errors in conventional column-parallel ADC are removed by well-known noise reduction method, correlated double sampling (CDS). However, in the developed DPS, the reset and signal data transfer paths are intricately interconnected within the cluster, leading to residual offset components that cannot be fully canceled out by the CDS operation.

There are three potential solutions to address the CL-FPN issue: 1) Minimizing parasitic capacitance – design the layout to avoid forming parasitic capacitors between the output nodes of adjacent ADCs, 2) CDS-based offset cancellation – integrate the SRAM for reset data and the SRAM for signal data into a single SRAM, thereby enhancing offset cancellation through the CDS operation, 3) adding a decoupling cap – as illustrated in Fig. 4, introduce a decoupling capacitor at the COMP node to reduce CL-FPN. This approach enhances the circuit's robustness against CL-FPN.

Next, the CL-XT phenomenon arises at the boundary between bright and dark regions. In this situation, the output code value of a dark pixel is influenced by that of an adjacent bright pixel, causing the dark pixel to be incorrectly interpreted as a white pixel. The underlying cause of the CL-XT issue is depicted in Fig 4. When PIX<A> is in a dark condition and PIX<C> is in a bright condition, the PIX<A> is normally converted and stored in the SRAM during A/D conversion periods for reset and signal. However, during the A/D conversion of

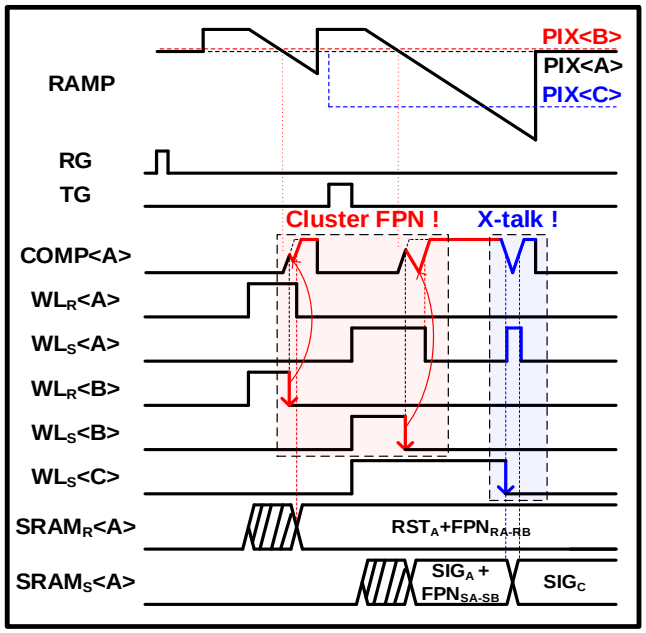
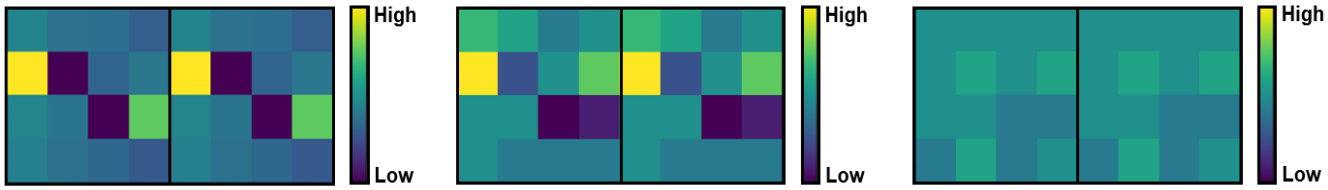


Fig. 4. The timing diagram of the causes of cluster-induced fixed pattern noise and cluster-induced cross-talk.



(a) (b) (c)

Fig.5 Cluster-type FPN results. (a) Measured result, (b) Simulated result with parasitic components, (c) Simulated result after optimizing the parasitic components.

PIX<C> in the bright condition, WL_S<C> parasitically couples to COMP<A>, affecting the output of PIX<A> and causing the CL-XT error. At that moment, the COMP<A> node temporarily transitions from a high level to a low level, causing the previously closed word-line transistor in the SRAM to re-open. As a result, the dark code stored in the SRAM is overwritten by a white code, and the dark pixel is erroneously converted into a white pixels, as if it were illuminated. This phenomenon is defined as CL-XT.

The CL-XT issue arises due to coupling between adjacent ADC output lines. There are two potential solutions to mitigate this problem: 1) minimizing parasitic capacitance – design the layout to prevent parasitic capacitors from forming between adjacent ADC output node, COMP, and SRAM input node, WL_S, 2) increasing the COMP node's high-level voltage after the decision time – this ensures that even if capacitive coupling occurs, the COMP node voltage does not fall below the logic threshold of the subsequent logic buffer. Consequently, the closed word-line remains closed, preventing the dark code from being overwritten by a white code. By implementing these solutions, the CL-XT issue can be effectively mitigated.

III. Simultion and Measurement Results

A 2-Mp, 4.95-µm pixel pitch GS CIS with pixel-parallel ADCs was implemented using 65 nm (top-substrate for pixel part) and 28 nm (bottom-substrate for logic part) CIS processes. The die micrographs of the top and bottom chips are shown in Fig. 6. The designed pixel-parallel ADC with M×N cluster structure was validated using SPICE circuit simulation and a netlist containing parasitic components after completing and verifying the cluster layout.

The CL-FPN simulation results are shown in Fig. 5. The root cause of the issue was thoroughly analyzed through circuit simulation (see Fig. 5(b)) and was resolved through layout optimization (see Fig. 5(c)). To further improve CL-FPN, a parametric sweep of the decoupling capacitor size at the COMP node was performed, as shown in Fig. 7. The simulation results indicate that increasing the decoupling capacitor size at the COMP node significantly reduces the CL-FPN value.

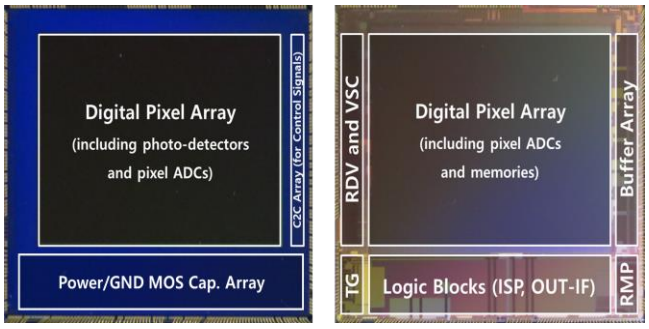


Fig.6 Chip micrographs (left: top chip, right: bottom chip).

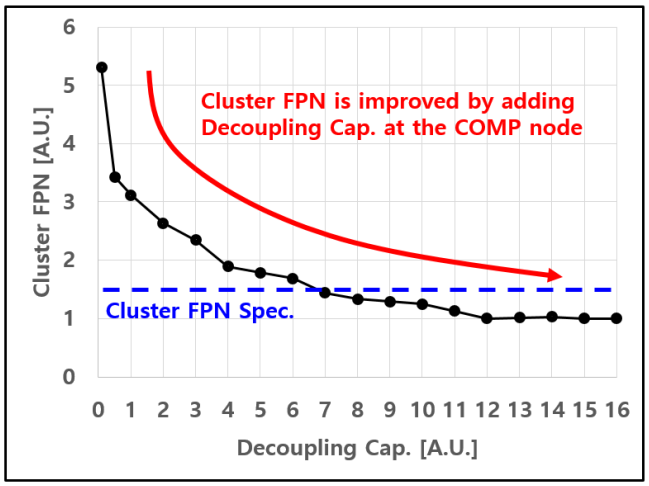


Fig.7 (a) The simulation results of sensor Cluster FPN as a function of the decoupling capacitor's size at COMP node

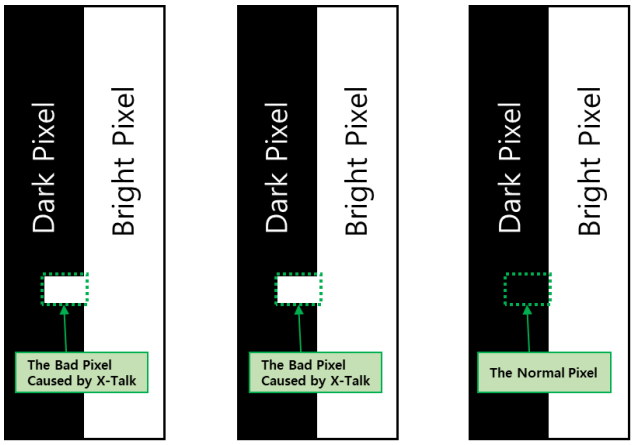


Fig. 8. Cluster-type Cross-Talk results. (a) Measured result, (b) Simulated result with parasitic components, (c) Simulated result after optimizing the parasitic components.

The CL-XT simulation results are presented in Fig. 8(a) and Fig. 8(b). To address the CL-XT issue, we optimized the parasitic capacitance and observed that the CL-XT problem was successfully mitigated, as demonstrated by the simulation results. Finally, we confirmed that all simulation results closely match the package measurements results of prototype DPS.

IV. CONCLUSION

The proposed CL-FPN and CL-XT reduction methods have been successfully demonstrated. Cluster-induced noise analysis is a critical approach for enhancing low-light performance and improving image quality under bright conditions. The DPS with pixel-parallel ADC is an advanced next-generation GS CIS, and its application is expected to expand across various fields in the future. We anticipate that as circuit design, device, and process technologies for digital pixel miniaturization continue to advance, the scope of DPS applications will further broaden.

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